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A Counter Architecture for Online Estimation of DVFS Profitability

Introduction

Dynamic Voltage and Frequency Scaling (DVFS) is a well-known and powerful technique for addressing a wide range of important problems in contemporary processors, including: reducing energy and power consumption, increasing performance (at the cost of increased power consumption), addressing timing errors due to process variability, enabling dynamic thermal management, and dynamic lifetime reliability management.
There are a number of methods to estimate the profitability of applying DVFS in a processor, such as proportional scaling, linear scaling, estimated linear scaling and stall cycle counting. However, these methods have several drawbacks, such as inaccuracy and the introduction of runtime performance and/or energy overhead.

Technology

Researchers at Ghent University have developed a hardware counter architecture to accurately estimate the profitability of DVFS in a processor. The counter architecture estimates what the impact is of scaling clock frequency and supply voltage on performance and energy consumption. The total execution time of a program running on a processor can be divided into a pipelined fraction subject to clock frequency and a non-pipelined fraction due to off-chip memory accesses. The counter architecture estimates these two fractions, from which DVFS profitability can be estimated: the pipelined fraction scales proportionally with clock frequency (e.g., decreasing/increasing clock frequency by a factor of 2, reduces/increases the pipelined fraction by a factor of 2) whereas the non-pipelined fraction does not scale at all. This yields an estimate for the execution time under DVFS, which in its turn is used to estimate energy consumption.

Applications

The proposed counter architecture is generally applicable across many processor types, going from embedded in-order processors to high-end out-of-order processors.

Advantages

- The counter architecture accurately determines the pipelined and non-pipelined fraction of the total execution time, providing higher accuracy than proportional scaling, estimated linear scaling and stall cycle counting.
- The counter architecture requires only one run at an arbitrary V/f point, thereby introducing less run-time overhead than a linear scaling approach.
- Very limited hardware cost to implement the counter architecture: 70 bits plus an incrementer.

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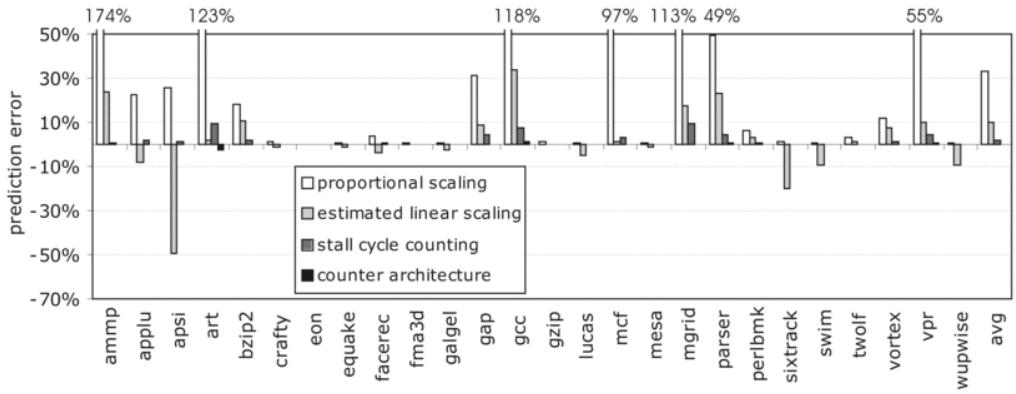
Status of development

The counter architecture was evaluated in a cycle-accurate architectural simulator, which models a processor in software. The proposed counter architecture was demonstrated to outperform previously proposed methods in terms of estimating the impact of DVFS on execution time, energy and energy-efficiency (i.e., energy-delay product and energy-delay-square product).

Intellectual property

European patent application EP10798285.2, filed on 10 December 2010
Granted US patent US8812808, filed on 10 December 2010, granted on 19 August 2014

Figure



Prediction error for predicting execution time at the 0.9 GHz operating point for proportional scaling, estimated linear scaling, stall cycle counting, and the proposed counter architecture.

The Inventors

Lieven Eeckhout, ELIS Department, Ghent University
Stijn Eyerman, ELIS Department, Ghent University

References

Stijn Eyerman and Lieven Eeckhout. A counter architecture for online DVFS profitability estimation. IEEE TRANSACTIONS ON COMPUTERS. Vol. 59. 2010. 1576-1583.

Keywords

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Contact

Piet De Vos, PhD, Licensing Manager, +32 9 264 79 61, Piet.Devos@UGent.be